Po-Shao Chen

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Education

Doctor of Philosophy in Electrical and Computer Engineering Sep. 2022 – Present
University of Michigan *Ann Arbor, Michigan*

Master of Science in Electronics Engineering Sep. 2018 – Feb. 2021
National Taiwan University *Taipei, Taiwan*

- Thesis: An Energy-Efficient Accelerator IC for Dark Channel Prior Based Blind Image Deblurring

Bachelor of Science in Electrical Engineering Sep. 2014 – June 2018
National Taiwan University *Taipei, Taiwan*

Journal Paper

P.-S. Chen, Y.-L. Chen, Y.-C. Lee, Z.-S. Fu, C.-H. Yang, "A 28.8mW Accelerator IC for Dark Channel Prior Based Blind Image Deblurring," *IEEE Journal Solid-State Circuits (JSSC)*, vol. 59, no. 6, pp. 1899-1911, June 2024.

Conference Papers

E. Dikopoulos, L. Wormald, Y.-T. Hsu, W. Tang, P.-S. Chen, Z. Zhang, M. P. Flynn, "A Relaxation Oscillator-Based Probabilistic Combinatorial Optimization Engine for Soft Decoding of LDPC Codes," *IEEE European Solid-State Electronics Research Conference (ESSERC)*, Sep. 2024

L.-H. Lin, Z.-S. Fu, P.-S. Chen, B.-Y. Yang, and C.-H. Yang, "A 4.8mW, 800Mbps Hybrid Crypto SoC for Post-Quantum Secure Neural Interfacing," *Int. Symposium on VLSI Circuits (VLSI Circuits)*, June 2023

P.-S. Chen, Y.-L. Chen, Y.-C. Lee, Z.-S. Fu, and C.-H. Yang, "A 28.8mW Accelerator IC for Dark Channel Prior Based Blind Image Deblurring," *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2021.

Honors & Awards

Master's Thesis Award, IEEE Taipei Section June 2022

Bronze Medal Award, Macronix Golden Silicon Award Aug. 2021

Research & Work Experience

Graduate Student Research Assistant Aug. 2022 – Present
LEAPS, University of Michigan *Ann Arbor, Michigan, USA*

Research Assistant Aug. 2021 – July. 2022
Digital Circuits and Systems Lab, National Taiwan University *Taipei, Taiwan*

- Delivered the oral presentation for blind image deblurring accelerator IC in *A-SSCC* 2021

Mandatory Military Service Apr. 2021 – July 2021
R.O.C. Army *Taiwan*

- Received rifleman's and tank ammunition loader's training

Graduate Student Researcher July 2018 – Mar. 2021
Digital Circuits and Systems Lab, National Taiwan University *Taipei, Taiwan*

- Designed blind image deblurring accelerator IC with **complete cell-based ASIC design flow**
- Applied the deblurring accelerator to Intel FPGA board for surgical image deblurring

- Implemented the algorithm for efficiently analyzing current signals from the sensor measuring the alcohol in gaseous state to determine the concentration

Undergraduate Student Researcher Mar. 2018 – June 2018
Digital Circuits and Systems Lab, National Taiwan University *Taipei, Taiwan*

- Analyzed blind image deblurring algorithms

Electrical Engineering Intern July 2017 – July 2018
HP *Taipei, Taiwan*

- Designed compact WLAN antenna for the narrower bezel laptop
- Applied Visual Basic for Application (VBA) in Excel to collect the WLAN antenna field trials' data and generate charts automatically
- Participated in the live stream for introducing the internship program

Selected Projects

Blind Image Deblurring Accelerator IC Sep. 2018 – Feb. 2021

- Implemented the chip having 2562x acceleration in full-HD image deblurring comapred to Intel i7-4790
- Achieved 4x higher normalized area efficiency and 7.5x higher normalized energy efficiency than the prior design
- Used less area than the state-of-the-art design despite supporting 4x larger image size and better capability of image deblurring

Gas Concentration Analysis Sep. 2018 – Dec. 2020

- Designed digital filters for raw signals from gas sensor with MATLAB
- Analyzed signals' patterns and constructed ideal signals to aid detection
- Reduced the run-time by 50% for gas concentration detection with remained accuracy

Stereo Matching Sep. 2018 – Dec. 2020

- Explored and implemented different algorithms to have the feasible stereo matching performance
- Modified algorithms with various pre-processing and post-processing methods to enhance stereo matching results

Skills

Programming Language: Verilog, SystemVerilog, MATLAB, Python, C/C++, Latex
Hardware Design Tools: NC-verilog, Verdi/nWave, Design Compiler, Innovus, Calibre, Altera Quartus, Virtuoso